

Application Serial No. 10/643,187 - Filed August 19, 2003

IN THE ABSTRACT:

Please amend the Abstract as follows.

A semiconductor device has multilevel memory cells, each cell storing at least three levels of data each. At least a first data composed of first data bits and a second data composed of second data bits are arranged in order that at least a bit of an N-order of the first bits and a bit of the N-order of the second bits are stored in one of the cells, the N being an integral number. A voltage corresponding to the N-order bits is generated and applied to the one of the cells in response to an address information corresponding thereto. Another semiconductor device has The multilevel memory cells are arranged so as to correspond to a physical address space, each cell storing 2^n levels of data each expressed by n ($n \geq 2$) number of bits (X_1, X_2, \dots, X_n). A logical address is converted into a physical address of the physical address space. Judging A judgement is made as to whether a logical address space including the logical address matches the physical address space. When matched, the most significant bit X_1 is specified once using by performing a single comparison operation using a reference value. The specified bit is output from one of the cells corresponding to the physical address. If not matched, the bits (X_2, \dots, X_n) are specified by a time specifying operation maximum using maximum n number of performing multiple comparison operations using different reference values. The data writing/reading operations to/from the semiconductor devices can be stored in a computer readable medium as program codes for causing a computer to execute these operations.